DBIT - DIRECT BACKSIDE INTERCONNECT TECHNOLOGY: A MANUFACTURABLE, BOND WIRE FREE INTERCONNECT TECHNOLOGY FOR MICROWAVE AND MILLIMETER WAVE MMICS

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ABSTRACT

A novel, highly manufacturable, low loss interconnect technique - DBIT (Direct Backside Interconnect Technology) - is presented. Polymer bumps are used to provide RF and ground interconnects between the backside of the MMIC chip and the substrate. The RF interconnects have been characterized up to 40 GHz. Measured interconnections have a 24 GHz bandwidth with 0.05 dB insertion loss at 10 GHz. This approach eliminates wire bonds which are known to introduce significant parasitics including a variable series inductance and which constraint the design of microwave MCMs and single chip packages.

INTRODUCTION

In recent years advances in the performance and manufacturability of GaAs MMICs and MCMs have resulted in their insertion into more and more military as well as commercial systems. One of the keys to this technology is the ability to reproducibly and reliably form interconnects between the MMIC chip and the substrate. Traditionally the RF and dc interconnects and control lines have been formed by wire or ribbon bonds. However, as system complexity increases and performance requirements become more stringent, traditional wire bonds exhibit several limitations. In particular, the highly variable parasitic reactance and conductor loss associated with wire bonds used for RF interconnects can result, at best, in variable performance and, in the worse case, to performance (gain) degradation. Bond wires are also a source of radiation and increased electromagnetic coupling. This situation reduces isolation and can cause oscillations in circuits with high gain blocks. These handicaps become particularly noticeable with increasing frequency where circuit performance is at a premium.

To address the limitations presented by wire bond interconnects, many different bond wire free interconnect schemes have been developed, including flip chip [1] and MHDI (Microwave High Density Interconnect) [2]. While each of these techniques addresses the limitations associated with wire bond technology, each is not without its own characteristic limitation. For example, current implementations of flip chip technology use coplanar or lumped element circuit topologies and pay the penalty of larger circuit area and less design flexibility when compared with microstrip topology.

In this work we introduce Raytheon's approach to a bond wire free chip interconnect technology: Direct Backside Interconnect Technology or DBIT. This interconnect technology is schematically illustrated in Figure 1. In the DBIT approach all RF, DC and

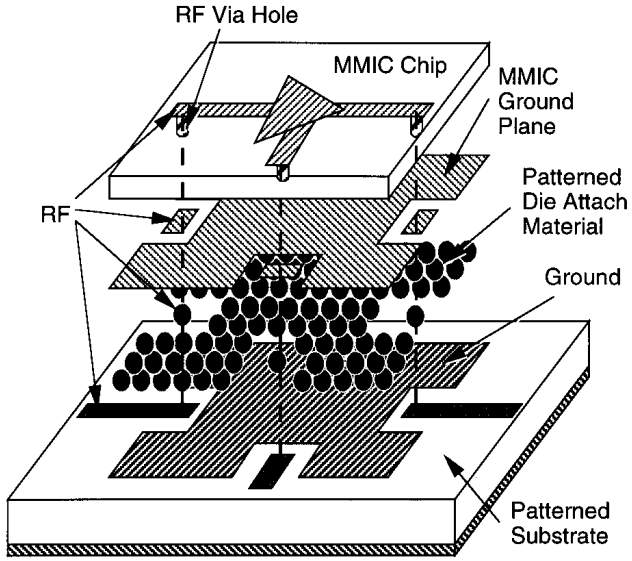

Figure 1: Schematic of the DBIT approach highlighting the interconnect via holes, patterned MMIC backside, patterned substrate and interconnect/die attach material. Note generic MMIC amplifier is shown with a microstrip layout topology.

0-7803-4603-6/97/$5.00 (c) IEEE

control signals are brought to the backside of thinned MMIC chips through via holes. The chip is then directly mounted onto a patterned substrate such that the RF, DC, control lines and ground plane mate with the respective features on the substrate. All chip connections are made in a single assembly step - the chip die attach step. The parasitic reactance and conductor loss associated with the DBIT RF interconnects are dominated by the impedance of the via hole and are predictable and highly repeatable. Since the DBIT approach uses thinned wafers, it is compatible with conventional microstrip circuit topology. In this work conventional 4 mil thick GaAs wafers are used, although any wafer thickness can be used provided through wafer via holes can be formed.

ASSEMBLY

The challenge in implementing the DBIT approach was to develop a viable, manufacturable die attach process. Solder preforms and dispensed materials (solder pastes, epoxies, thermosets or thermoplastics) - materials commonly used for the mounting of conventional MMIC chips to substrates - are not compatible with the DBIT process. Rather, in order for DBIT to be successful the die attach medium must be patterned to match the metal pattern on the back of the MMIC chip such that when the chip is mounted to the carrier the die attach layer does not cause electrical shorts to occur between the different signal lines and ground plane.

In order to develop a patterned die attach layer, different "bump" technologies and materials were evaluated, including polymer bumps and solder bumps. Application of the bump layer to the backside of the MMIC, to the frontside of the substrate, and a combination of both were considered. While DBIT assemblies were successfully fabricated with each of these techniques and materials, the simplest and most reproducible results to date were achieved using stenciled conductive epoxy bumps. The bump pattern was formed using commercially available stencils and screen printers. In this work a precision flip chip aligner was used to align the chip to the substrate. However, in a manufacturing environment a conventional pick and place assembly tool can we used to provide accurate die placement. An example of the completed assembly is shown in Figure 2.

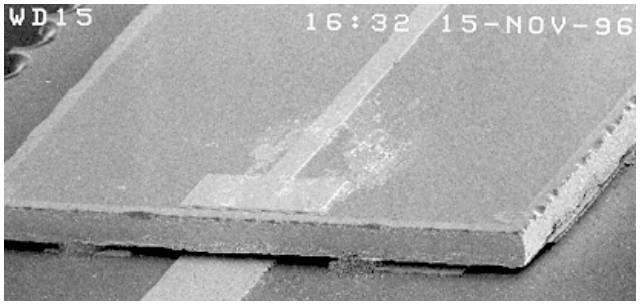

Figure 2: Scanning electron micrograph of the DBIT test chip mounted on a patterned alumina carrier with silver loaded epoxy bumps

To date DBIT test structures have been successfully assembled using polymer bumps formed with several different types of commercially available silver loaded conductive epoxy materials. These include epoxies that have previously been qualified for use as die attach material in Raytheon's production MMIC assembly line for low power dissipation applications. These epoxies have passed MIL-STD 883, method 5011 testing, including volume resistance, pre- and post- 1000 hour thermal aging at 150°C and environmental testing (thermal shock, temperature cycling, mechanical shock, random vibration and constant acceleration). Epoxy test structures - simple 50Ω transmission lines with a backside ground plane mounted with these epoxies to a metal base - were characterized from 0.3 to 20 GHz before and after environmental conditioning. The relative insertion loss of the epoxy test structures was found to be comparable to the loss of similar lines mounted with 80/20 AuSn solder. [3]

Environmental testing of DBIT test structures is

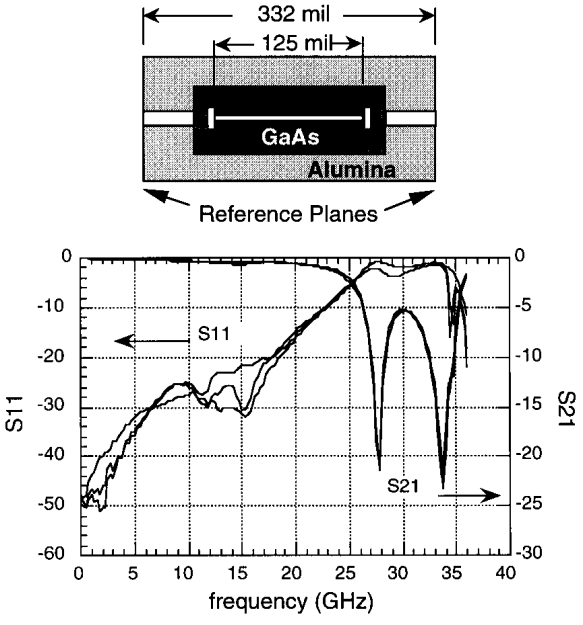

Figure 3: (a) Schematic of DBIT test structure. (b) A plot of |S21| and |S11| versus frequency for 3 DBIT test structures (de-embedded data).

currently underway. Preliminary results reveal no significant change in the test structure RF characteristics after temperature cycling.

RF CHARACTERIZATION

The DBIT RF test structures were simple 50Ω microstrip through lines on 4 mil thick GaAs. The ground substrate is 10 mil thick Alumina. The DBIT test structures were measured from 0.250 GHz to 36 GHz using an HP8510C network analyzer. A de-embedding procedure was used to remove the effect of connectors and test fixtures.

A plot of |S21| and |S11| versus frequency for the DBIT test structures is presented in Figure 3. The data shows very low insertion loss per DBIT transition as listed in Table 1. It should be noted that the curves presented in Figure 3 represent measurements on 3 different test structure assemblies and highlight the reproducibility of this interconnect approach.

Examination of the test data reveals that the test structure bandwidth is limited at the upper end by sharp transmission dips at 27.7 GHz and 33.7 GHz. In order to understand if this is a fundamental limitation of the DBIT interconnect additional characterization was performed.

Figure 4 shows measured $|S_{21}|$ data versus frequency for: (1) a DBIT through line; and (2) the patterned alumina substrate without the GaAs chip. As evidenced by the matching peaks of the second trace, the dips originate in the alumina substrate metallization. Although the frontside ground plane metallization or conductive patch is successfully grounded at low frequency, resonances appear above 25 GHz as the dimensions of areas not overlapping ground vias become a significant fraction of the wavelength. The resonant frequencies and the associated natural modes of oscillation are similar to those of a patch antenna with shorting pins. The resonances appear as stop bands in the ground path and thus severely affect the ability to ground the MMIC chip properly. Similar effects for wire bonded multichip modules have been observed by other researchers [4] and at Raytheon.

To further investigate the characteristics of DBIT, the substrate metallization pattern was analyzed up to 40 GHz using two different electromagnetic simulation tools, Sonnet and HP Momentum. Both CAD tools are based on the full wave solution of Maxwell's equations and the method of moments.

In Figure 5, the S-parameters of the patterned substrate simulated using Momentum reveal the same resonances seen in the measurement. The EM simu-

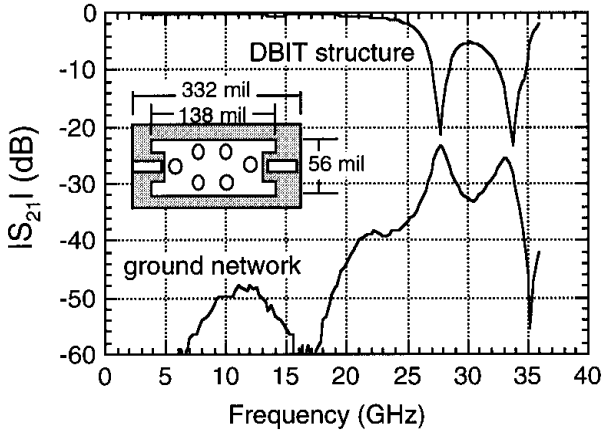

Figure 4. Measured de-embedded $|S_{21}|$ of DBIT through line and of underlying alumina substrate without top substrate. Reference plane at the signal line vias. Insert shows substrate metallization pattern and position of vias.

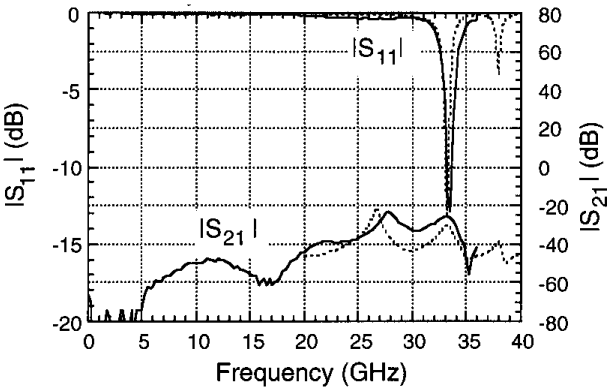

Figure 5. Measured (solid line) and EM simulated (dashed line) S-parameters of bottom substrate.

Table 1. Insertion loss of DBIT transitions.

	5 GHz	10 GHz	15 GHz	20 GHz	
loss of de-embedded test sample	0.18	0.28	0.46	0.54	dB
microstrip loss	0.11	0.17	0.22	0.25	dB
loss per DBIT transition	0.03	0.05	0.12	0.14	dB

lation gives close prediction of the performance over the entire frequency range considered. Visualization of the resonant mode patterns using SONNET shows a very large charge density in the corners of the conductive patch and a high current density near the closest via to ground at each resonant frequency. The onset of resonances is successfully pushed above 40 GHz when four vias in the corners of the patch and one in the center are added, as seen in the simulations of Figure 6.

The result of these measurements and simulations indicate that the limitations in the bandwidth of the DBIT test structures are due to resonances in the underlying substrate determined by the density of the vias and the substrate permittivity and not due to fundamental limitations of the DBIT approach.

On the basis of these observations, new substrates with different via configurations have been designed with the goal of extending the bandwidth of the DBIT transition to frequencies greater than 40 GHz. These structures will be used to determine the applicability of DBIT to millimeter wave systems.

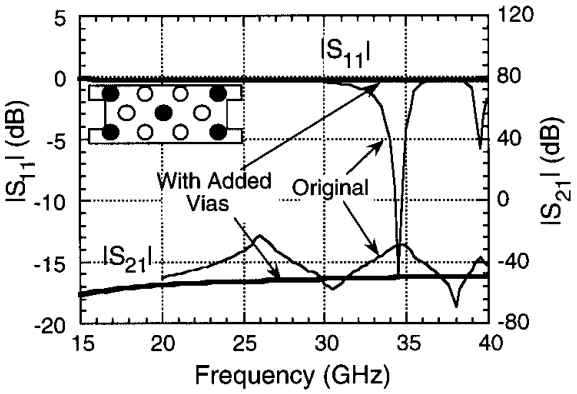

Figure 6. Simulated performance of bottom substrate with original via pattern and with added vias. Insert shows positions of additional vias

CONCLUSION

The data presented in this paper indicate that DBIT is a viable, reproducible, low loss, bond wire free interconnect technology suitable for addressing current and future single chip and multichip modules packaging needs. Measurements and simulations indicate that the frequency performance of the DBIT test structures is limited by resonances associated with the substrate material and grounding via hole configuration and is not a fundamental limitation of the DBIT approach. EM simulations suggest that by optimizing the design of the substrate bandwidths exceeding 40 GHz can be achieved. These results indicate that the application of DBIT can easily be extended to millimeter systems.

A 19-21 GHz multistage LNA MMIC and a 19-21 GHz 4 bit phase shifter / 1 bit attenuator with DBIT transitions are currently being fabricated.

ACKNOWLEDGMENTS

The author would like to acknowledge the assistance of the following people: S. Cain, M. Grigas for fabrication of the DBIT chips and W. Donovan for assembly. The authors will also like to acknowledge J. Lampen, P. Setzko and M. Kisner for early discussions on the development of the DBIT approach.

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